

P2010-B01

75W/80W/100W GK107/GK106/GM107 128-BIT GDDR5 in x32/x16 MODE
DVI-I-DL + DVI-D-DL/HDMI + mHDMI/DP



MICRO-STAR INT'L CO.,LTD

MS-V310

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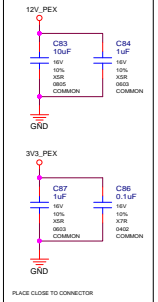
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NV_PN	600-12010-BASE-QS1		
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PCI Express



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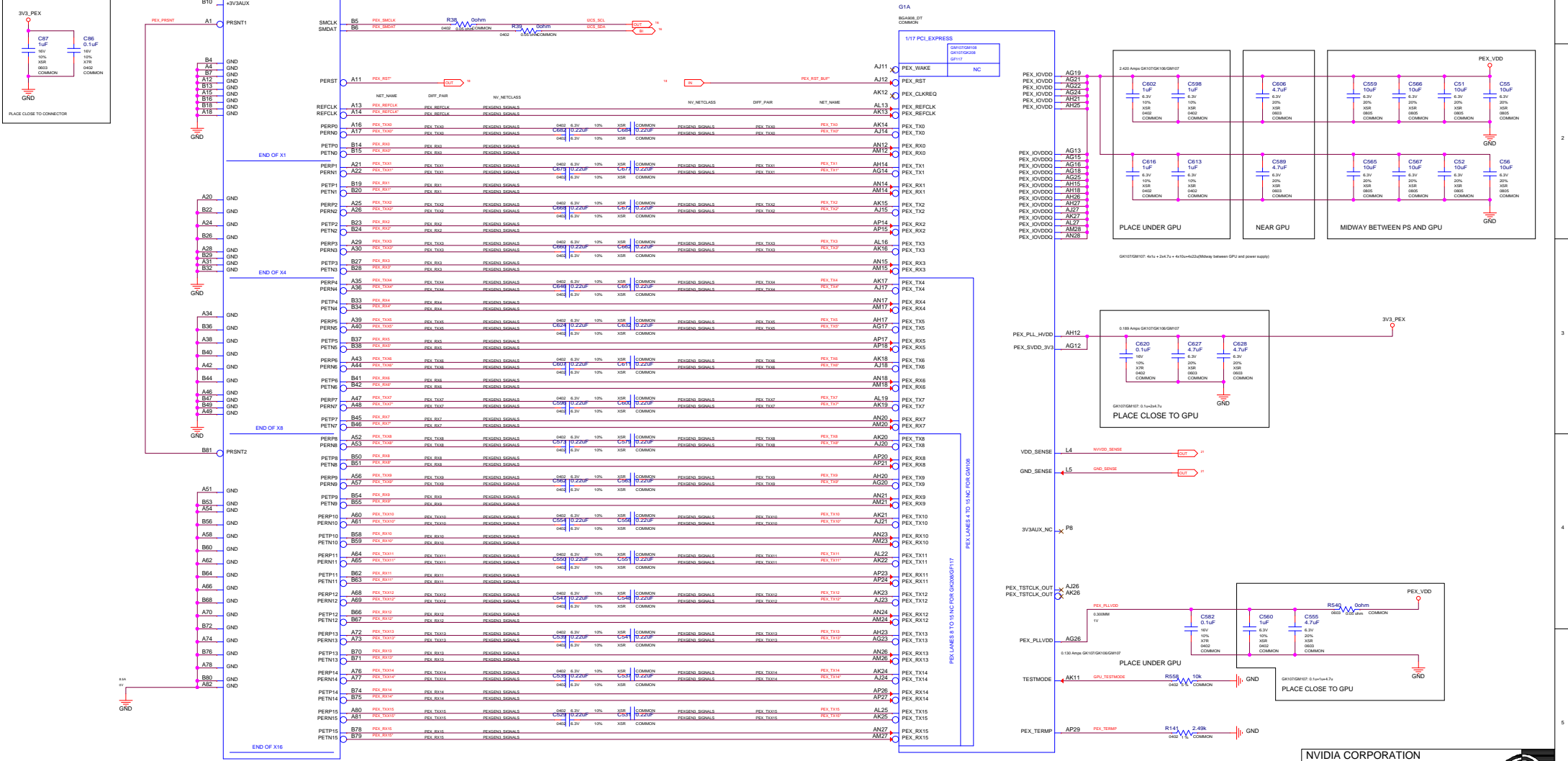
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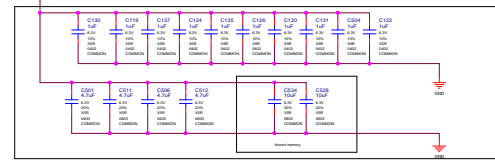
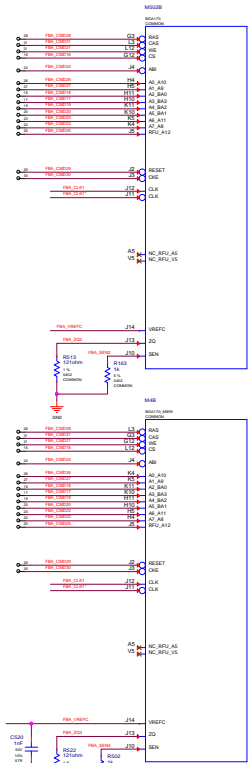


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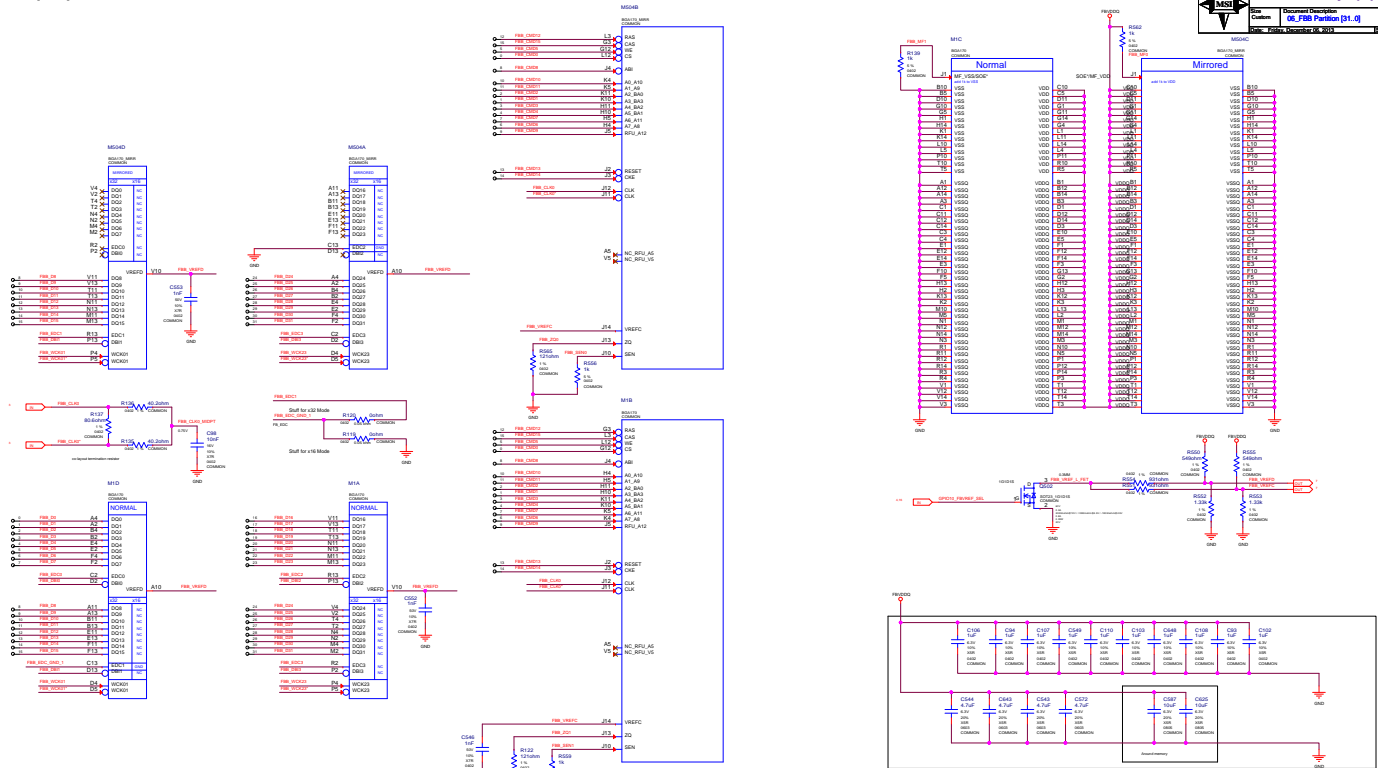


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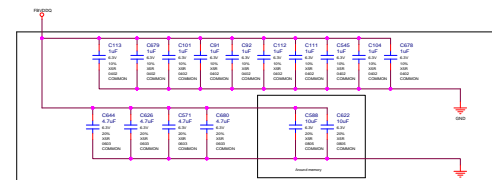
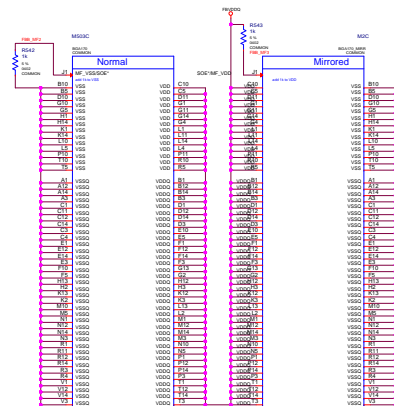
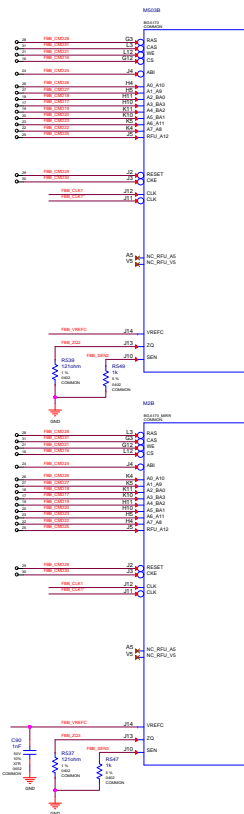
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1	FBB_D0-192	FBB_D0-192	FBB_D0-192
1	FBB_D0-193	FBB_D0-193	FBB_D0-193
1	FBB_D0-194	FBB_D0-194	FBB_D0-194
1	FBB_D0-195	FBB_D0-195	FBB_D0-195
1	FBB_D0-196	FBB_D0-196	FBB_D0-196
1	FBB_D0-197	FBB_D0-197	FBB_D0-197
1	FBB_D0-198	FBB_D0-198	FBB_D0-198
1	FBB_D0-199	FBB_D0-199	FBB_D0-199
1	FBB_D0-200	FBB_D0-200	FBB_D0-200



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INV_PN 600-12010-BASE-QS1			
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[illegible]

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REL-CD02	6	REL-CD11	6	REL-CD06	6
REL-CD03	6	REL-CD12	6	REL-CD07	6
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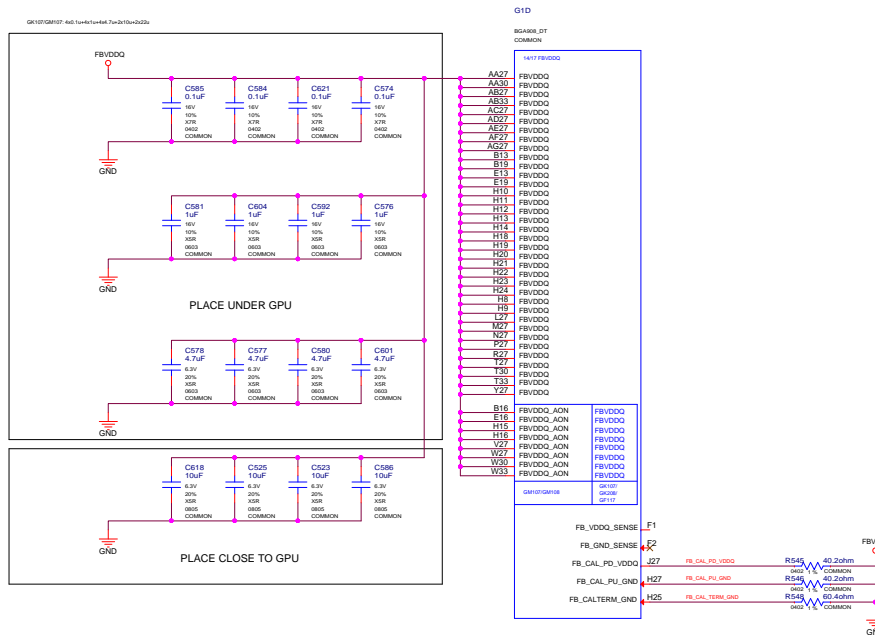
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GPU FB Decoupling




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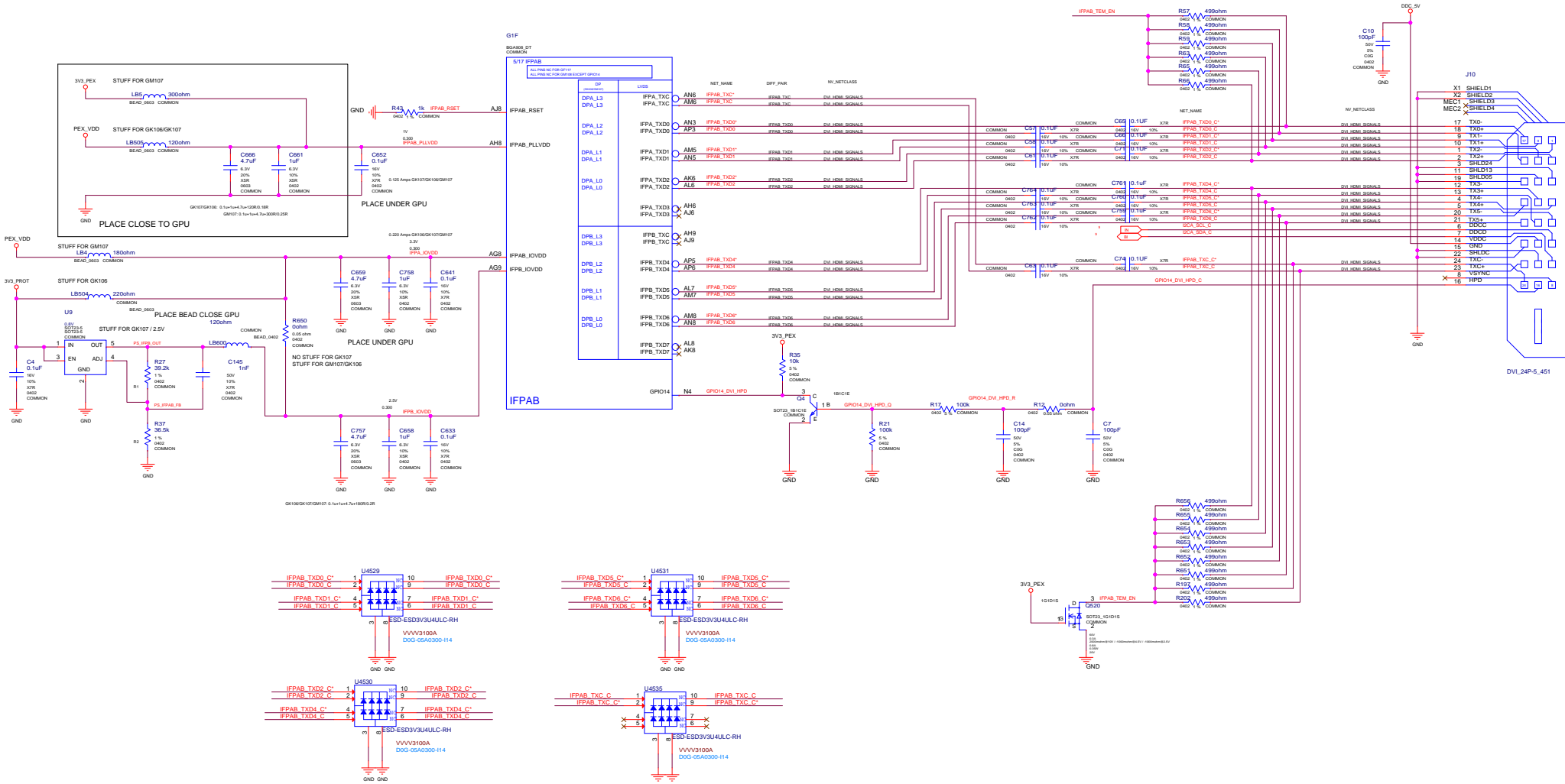
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IFPAB TMDS

LDO options		VOUT = VREF*(R1+R2)/R2
Option 1: TP523201CDB @ 1% Tolerance	TP523201CDB Internal VREF = 1.2V	$2.5V = 1.2V \times (R1 + 0.5925) / 0.5925$ $2.7V = 1.2V \times (R1 + 0.625) / 0.625$
Option 2: EM1105 @ 1.5% Tolerance	EM1105 Internal VREF = 0.8V	$2.5V = 0.8V \times (R1 + 0.9091) / 0.9091$ $2.7V = 0.8V \times (R1 + 0.9375) / 0.9375$
2.5V output Power dissipation = 0.168W @ 3.3-3.25uA/20mA		

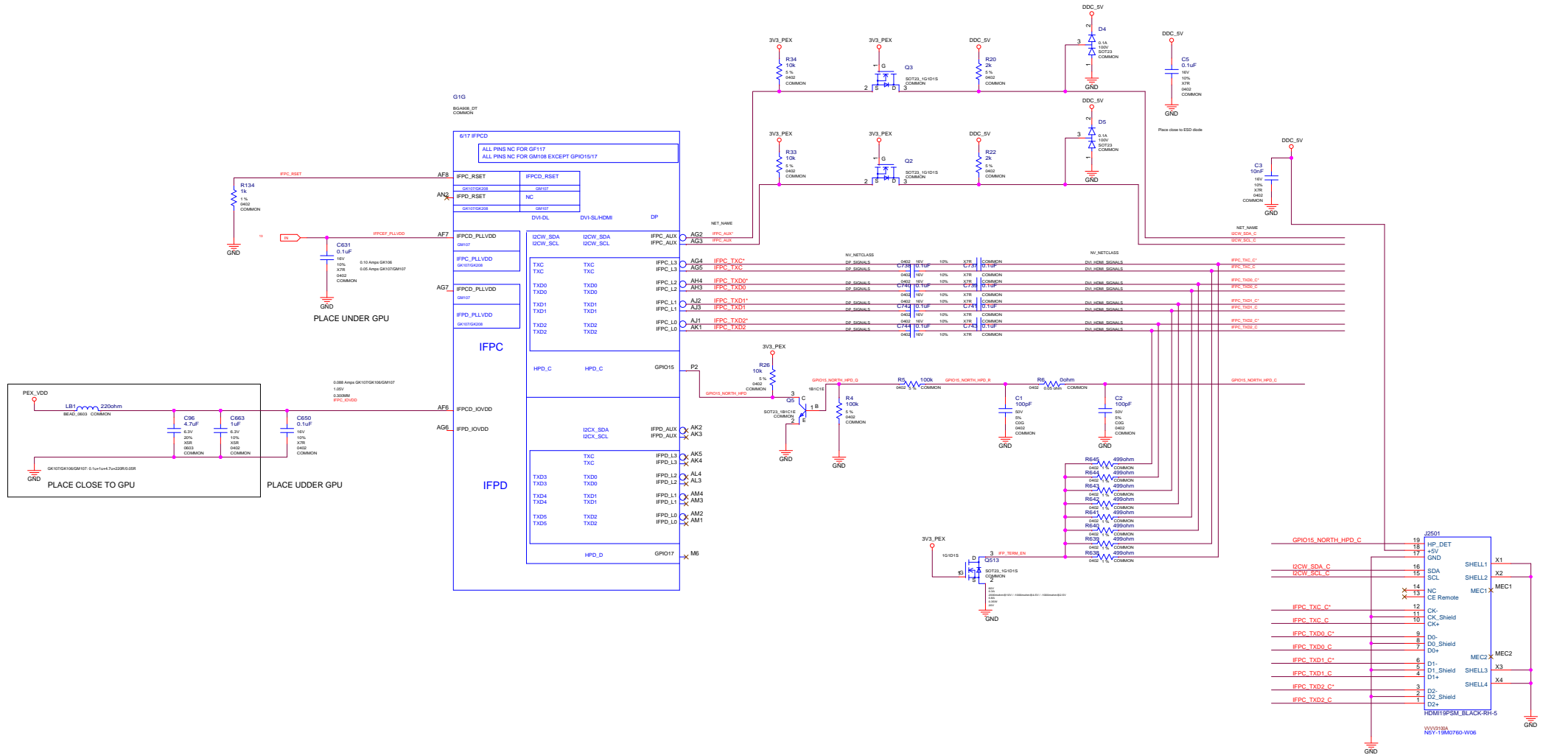


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BOM REV	A	DATE	28-OCT-2013

GPU Core Decoupling, GPU_VDD_3V3

MSI

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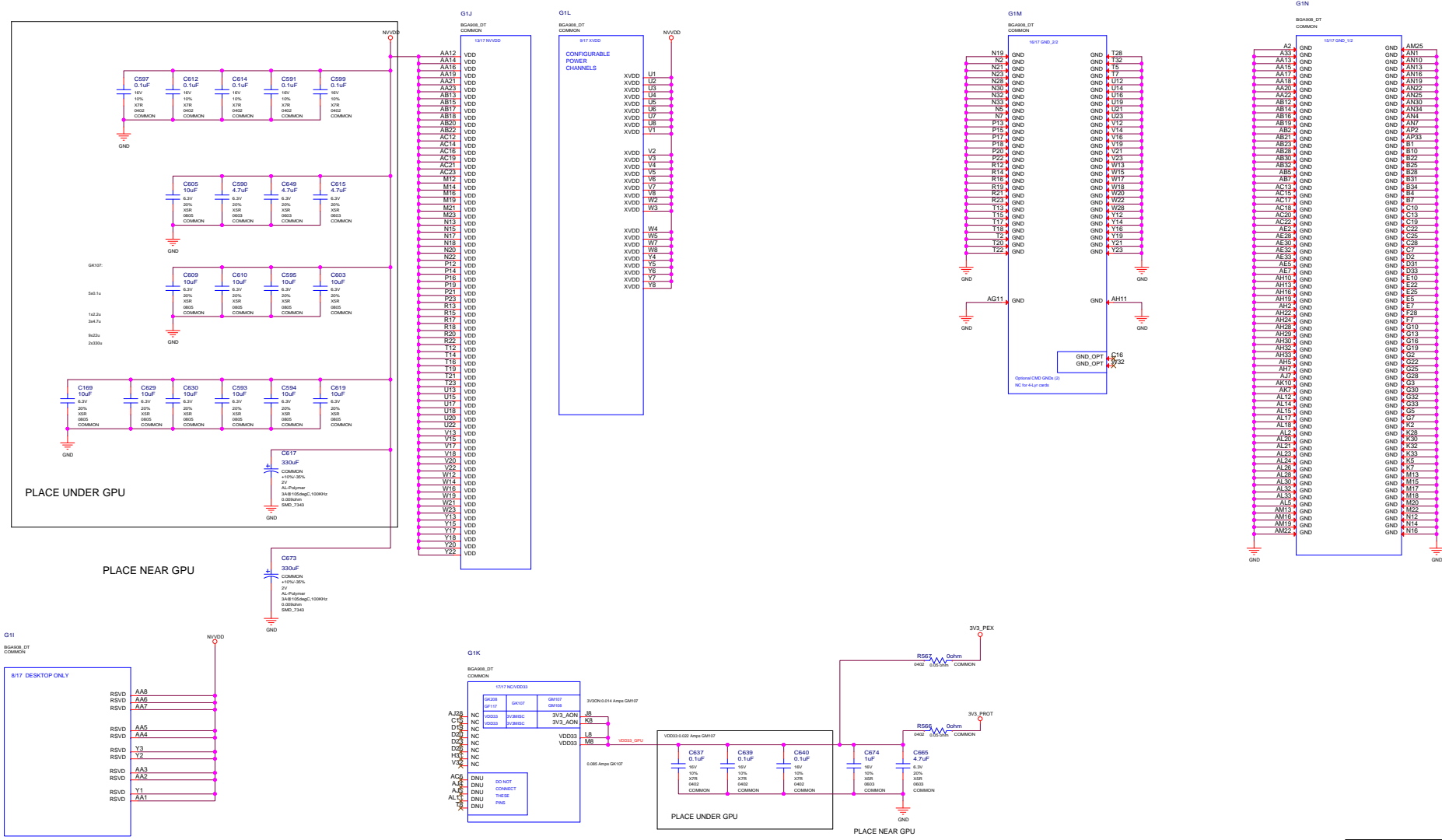
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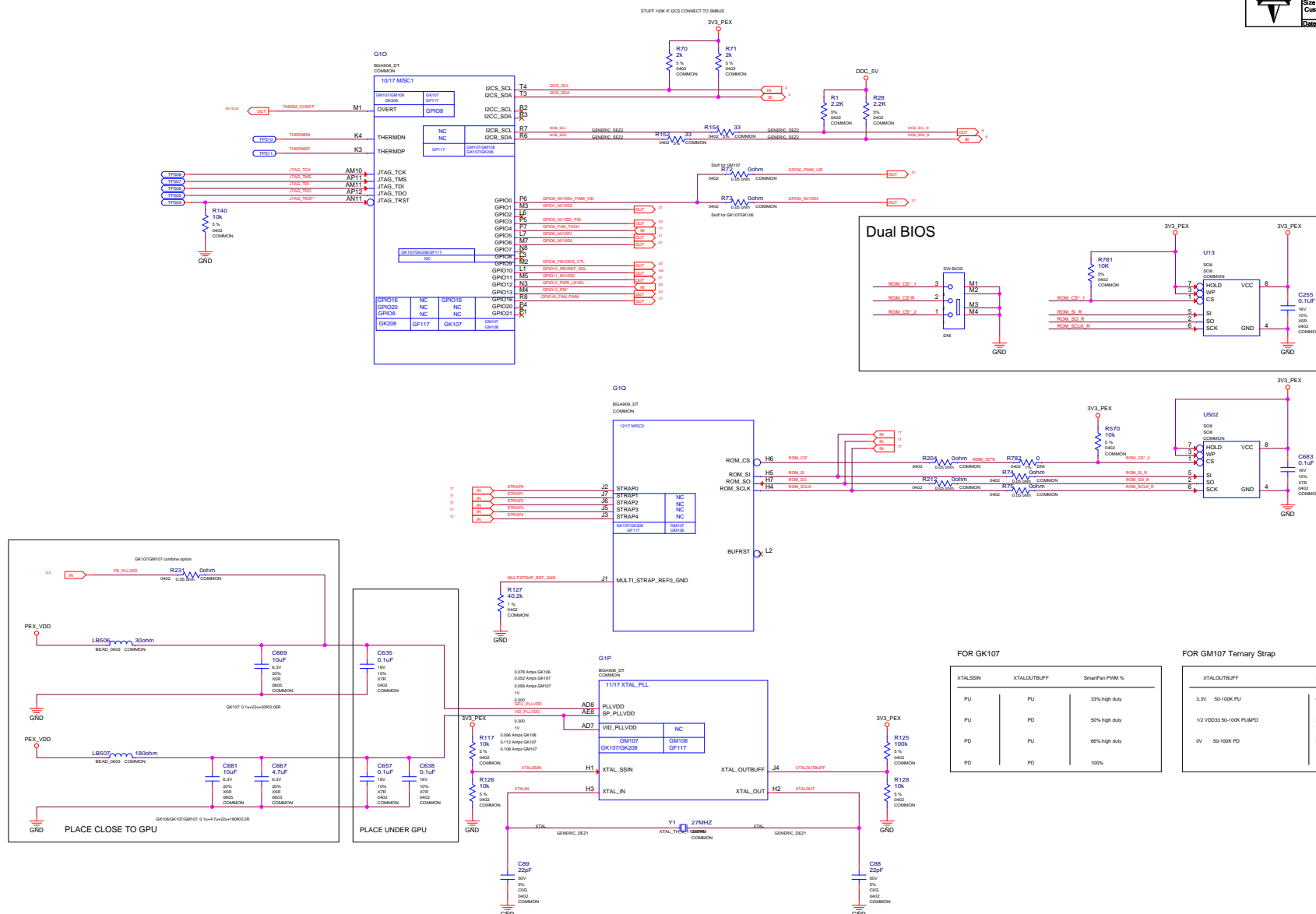
Rev 10

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Misc Interfaces



	MICRO-STAR INT'L CO.,LTD			
	MS-V310			
	Size Custom	Document Description 14_Misc Interfaces		Rev 1
Date: Friday, December 06, 2013		Sheet	1 of	21

XTALSSN	XTALOUTBUFF	SmartFan PWM %
PU	PU	33% high duty
PU	PD	50% high duty
PD	PU	66% high duty
PD	PD	100%

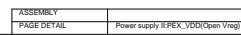
XTALOUTBUFF	SmartFan PWM
3.3V 50-100K PU	66% high duty
1/2 VDD33 50-100K PU&D	33% high duty
0V 50-100K PD	DISABLE


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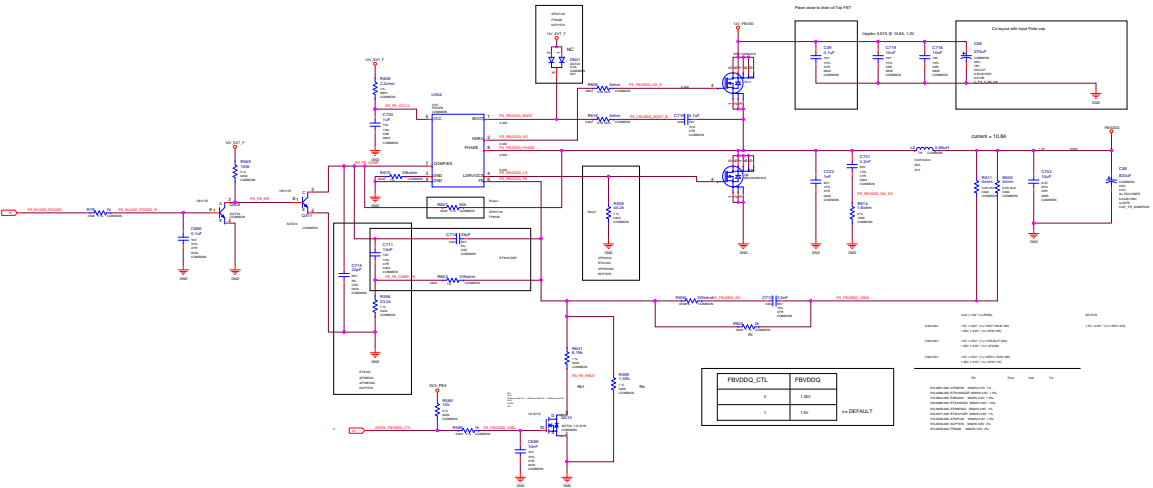


NV_PN	600-12010-BASE-QS1		
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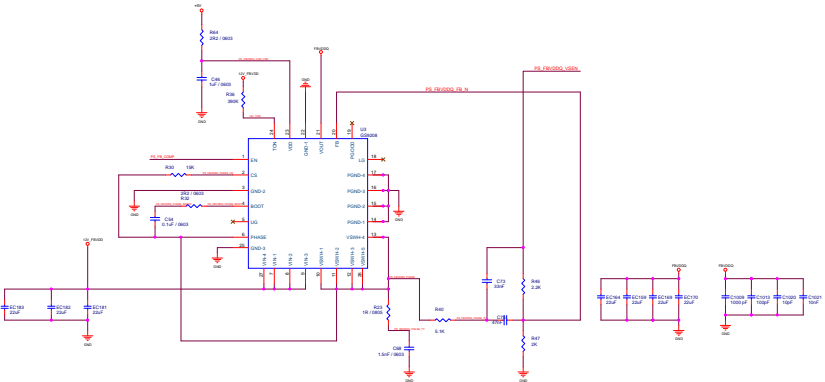
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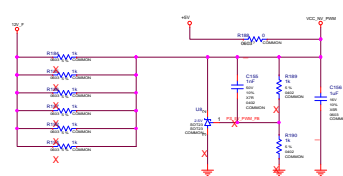
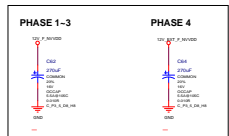


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NVIDIA CORPORATION	
NVIDIA Tegra 3 (T3024) (T3024)	
NVIDIA Tegra 3 (T3024) (T3024)	
Part No.	600-12010-BASE-QS1
Rev.	1.0
Doc No.	600-12010-BASE-QS1
Doc Rev.	1.0

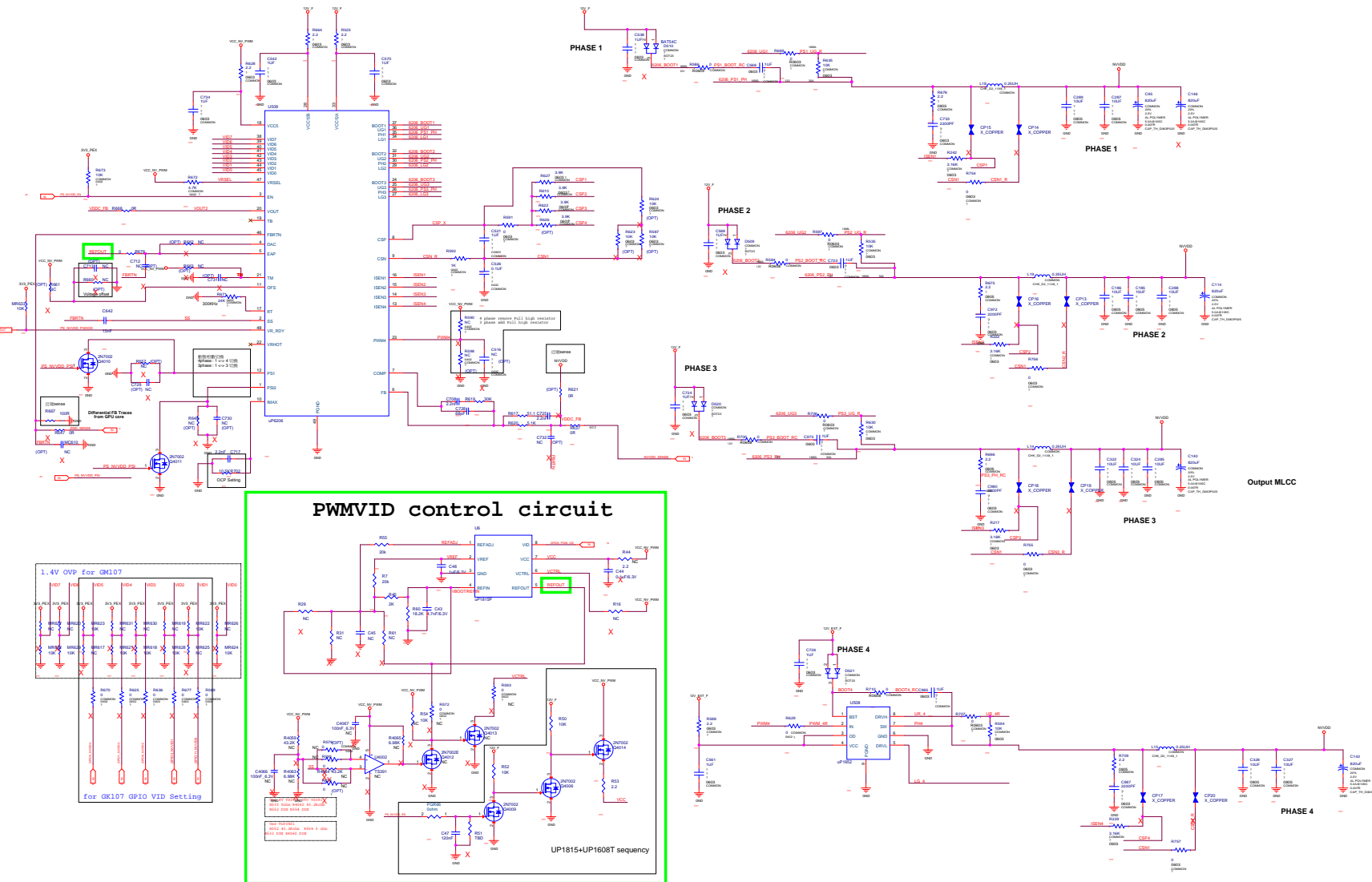




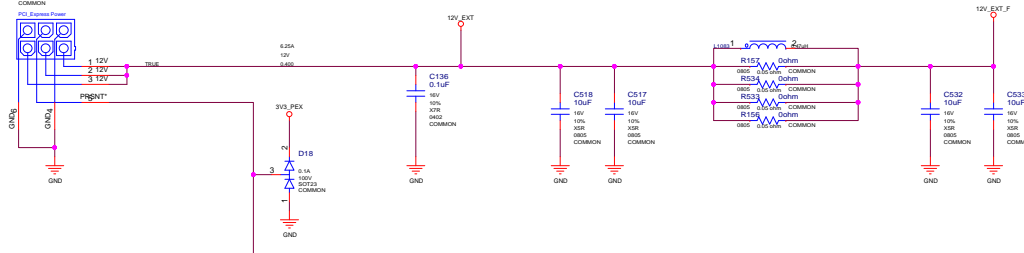
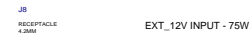
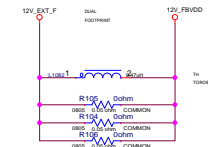
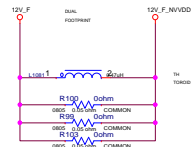
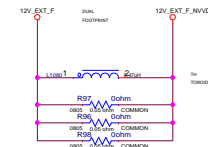
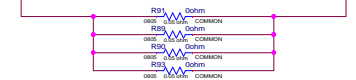
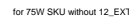
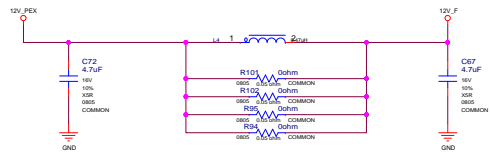
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	0	0	0	0	0	1.00E-07
	0	0	0	0	0	1.00E-06
	0	0	0	0	0	1.00E-05
	0	0	0	0	0	1.00E-04
	0	0	0	0	0	1.00E-03
	0	0	0	0	0	1.00E-02
	0	0	0	0	0	1.00E-01
	0	0	0	0	0	1.00E+00
	0	0	0	0	0	1.00E+01
	0	0	0	0	0	1.00E+02
	0	0	0	0	0	1.00E+03
	0	0	0	0	0	1.00E+04
	0	0	0	0	0	1.00E+05
	0	0	0	0	0	1.00E+06
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	0	0	0	0	0	1.00E+65
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TWO phase selection :

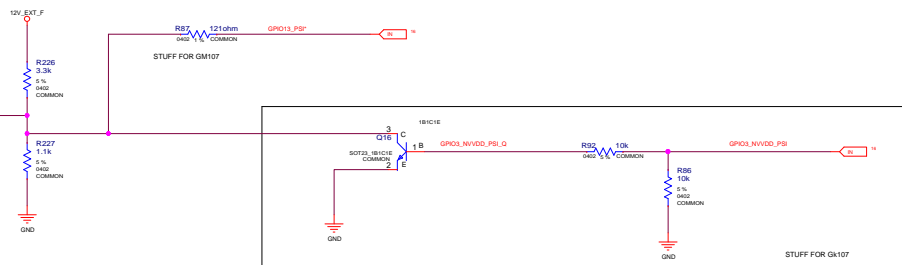
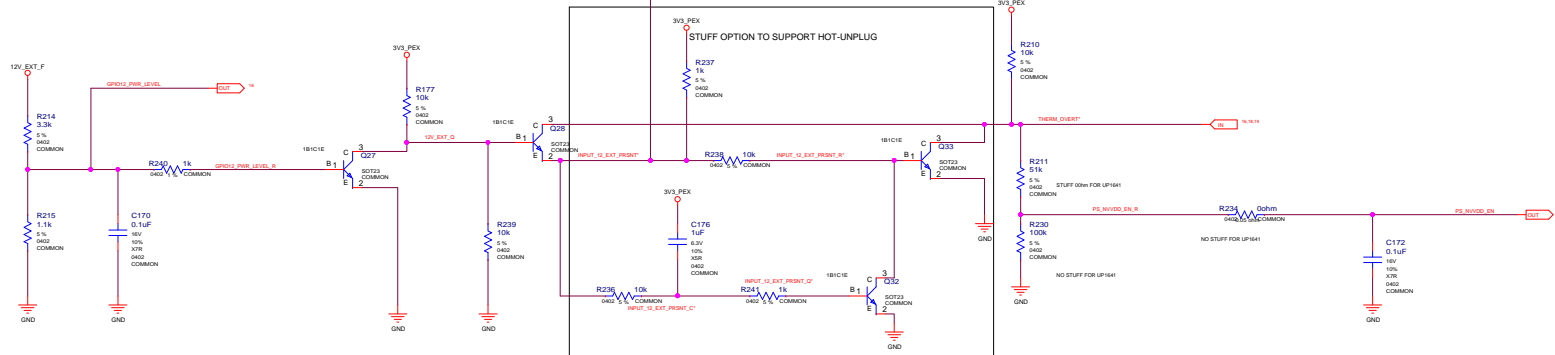
1. use ISEN1 & ISEN3 (ISEN2 & ISEN4 floating)
2. floating PWM4 & PSI2 (PSI1 to GND)
3. PH2 to GND
4. layout sequence TOP to BOTTOM : phase4 -> 3 -> 1 -> 2 , use phase1 &



PEX_12V INPUT - 66W



GPIO12_LOW_PERF*	GPU SPEED
0	SLOW
1	NORMAL



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	12V EXT / 12V PEX Power Select Circuit

Thermal, Mechanical



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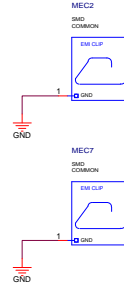
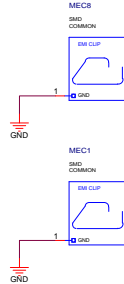
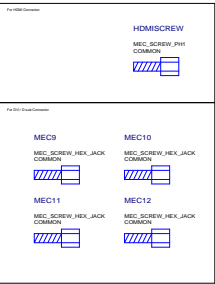
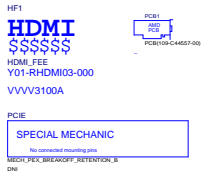
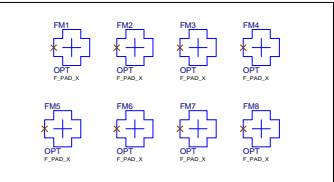
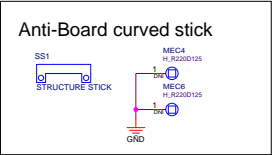
Size Custom

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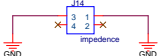
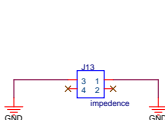


STACKUP IMPEDANCES - 607-12010-1000-B01.pdf

(Impedance Tolerance = +/- 10% unless otherwise noted)

Single Ended	SEZ	LW	Ref(above)	Ref(below)
TOP	40.0	0.17		L2
TOP	47.0	0.126		L2


Differential (Edge)	DEZ	SEZ	PriWidth	PriGap	NeckWidth	NeckGap	Ref(above)	Ref(below)
TOP	80.0		0.12	0.101				L2
TOP	90.0		0.1	0.12				L2



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ASSEMBLY	Thermal, Mechanical
PAGE DETAIL	